AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 29 as follows:

A prior art scan flip-flop circuit is constructed by a selector circuit operated by a selection signal, a master latch circuit clocked by a clock signal, and a slave latch circuit clocked by the clock signal (see: JP-A-1-96573). This will be explained ~~late~~ later in detail.

Please amend the paragraph beginning at page 4, line 13 as follows:

In a usual operation mode, the selection signal SEL is low (="0"), so that the combination circuit 1, the scan flip-flop circuit 4, the combination circuit 2, the scan flip-flop circuit 5 and the combination circuit 3 are electrically connected in series between the data input terminal D_{in} and the data output terminal D_{out}.

Please amend the paragraph beginning at page 4, line 19 as follows:

On the other hand, in a test operation mode, the selection signal SEL is high ="1"), so that the scan flip-flop circuit 4, the combination circuit 2 and the scan flip-flop circuit 5 are electrically connected in series between the scan-in terminal S_{in} and the scan-out terminal S_{out}. As a result, a so-called scan path is realized between the scan-in terminal S_{in} and the scan-out terminal S_{out}.

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